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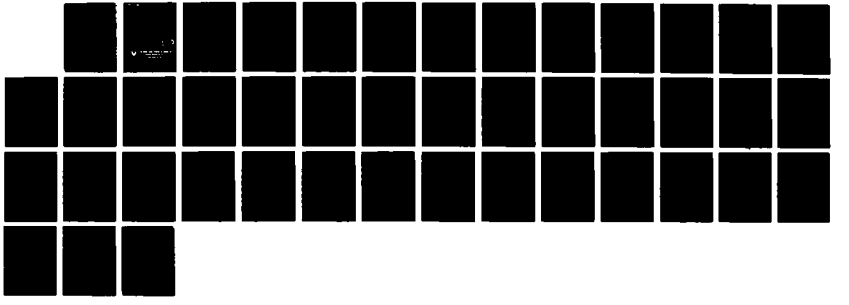

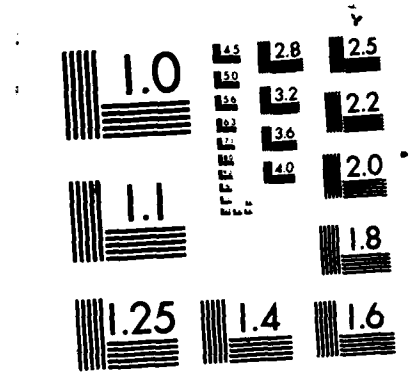

TECHNICAL REPORT ARIMD-TR-87001

AUTOMATED SEMICONDUCTOR MODELING

JOHN P. TOBAK

MAY 1987

US ARMY ARMAMENT MUNITIONS & CHEMICAL COMMAND
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A procedure is presented for the automatic creation of diode and transistor models used by the circuit and systems analysis computer program SUPER*SCEPTRE. A Hewlett Packard 9816S microcomputer and 4145B semiconductor parameter analyzer are used to control the process.

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INTRODUCTION

The circuit and systems analysis program SUPER*SCEPTRE is a powerful and highly interdisciplinary simulation language. Among its various attributes is its ability to utilize user defined models as circuit or system elements. This report describes a procedure for automating the creation of diode and bipolar transistor (NPN) models used by SUPER*SCEPTRE. While the final models generated appear in SUPER*SCEPTRE format, they can be easily adapted to the format of any nonlinear circuit simulation program. The modeling procedure mentioned begins with the acquisition of semiconductor data by means of an automated test setup. The setup is controlled by a Hewlett Packard 9816S microcomputer in concert with an H.P. 4145B semiconductor parameter analyzer. The data is then transformed by the 9816S into a SUPER*SCEPTRE model. A discussion of the parameters used to describe each model will first be presented followed by a description of the test configurations used to collect parameter data.

DIODE MODEL

The diode model for which the following parameters will be developed is taken from reference 1 and appears in figure 1. Diode model parameter definitions are:

CD = The sum of the diode transition and diffusion capacitances where:

$$\text{Transition capacitance} = \frac{Co}{(PHI - V_{CD})^{N}} = CJ$$

and

$$\text{Diffusion capacitance} = KD\ (JD + I_S)$$

JD = Current generator representing the diode junction current. This generator is a function of the voltage V_{CD}.

$$JD = I_S\ [EXP(\text{Theta}\ V_{CD}) - 1]$$

I_S = Diode reverse saturation current

Theta = Constant of the diode equation

RB = Diode bulk resistance

Co = Constant of the transition capacitance equation

PHI = Junction contact potential

N = Junction grading constant

KD = Diffusion capacitance constant = $\frac{\text{Theta}}{(6.28\ F)}$

F = Frequency parameter

V_{CD} = Voltage across capacitor CD, which is equal to the diode junction voltage

Diode Equation Constant and Reverse Saturation Current

The diode equation constant Theta is defined as

$$\text{Theta} = \frac{q}{(k\ T)} \tag{1}$$

where q is the charge of an electron, k is Botzman's constant, and T is the diode's junction temperature in Kelvins. Theta is obtained from the diode junction's measured forward biased characteristic and the assumption that the characteristic can be closely approximated by

$$JD = I_S\ EXP\ (\text{Theta}\ V_{CD}) \tag{2}$$

where I_S represents the diode's saturation current and V_{CD} its forward junction voltage. Diode D's forward characteristic is measured by using figure 2. The forward junction current and the foward junction voltage are recorded by means of source/monitor units SMU3 and SMU1, respectively, for automatically varied current values of SMU1. Source/monitor units are an integral part of the HP4145B and act as either voltage sources and current monitors or current sources and voltage monitors. In this test, SMU1 consists of a current source in parallel with a voltage monitor, while SMU3 acts as a zero voltage source in series with a current monitor. Physical connections between the diode under test and the HP4145B take place by means of an HP16058A test fixture. The fixture and its connections for the diode case are depicted in appendix A. The typical range of measurements taken are shown in figure 3.

Once obtained, measured data is submited by means of an HPIB (IEEE-488) interface to a computer program on the Hewlett Packard 9816s microcomputer. The program fits a curve of the form of equation 2 to the data yielding values for Theta and I_S. The curve fitting method used is described in appendix B. A comparison plot between typical measured data and its resulting fitted curve is shown in figure 4.

Bulk Resistance

Bulk resistance (RB) is obtained from the horizontal difference between the curves of figure 4 for high values of junction current. The migration of measured data to the right of the fitted diode equation is due to the forward voltage drop across RB and can be computed from figure 4 as,

$$RB = \frac{V_{dif}}{I} \tag{3}$$

The data used to fit the curve does not include the last few points of measure data. This is done to separate the effects of Rb from the proper determination of parameters Theta and I_S as well as legitimizing the calculation of RB by means of equation 3.

Leakage Resistance

Leakage resistance (RS) is obtained from the inverse slope of a curve fit (app B) of the diode's reverse leakage current versus its reverse bias voltage. The following is the assumed form to which the data is fitted:

$$I = \frac{V}{RS} \tag{4}$$

The circuit used to obtain the reverse bias data is demonstrated in figure 5. Voltage V is measured across SMU1 while current I is measured by SMU3. Except for the direction of the current generated by SMU1, figure 5 is identical to figure 2. The H.P. 9816S regulates the measurement taking procedure by applying typical currents on the order of a nanoampere and voltages as high as 40 volts.

Diffusion Capacitance Constant

Constant KD is obtained from storage time measurements collected using the circuit of figure 6. A periodic positive and negative pulse is applied to the diode's junction. Forward and reverse values of junction current (I_F and I_R, respectively) are recorded along with the time (t_s) needed for the junction to discharge and begin to recover to its steady state reverse saturation current (I_S). The current seen through the scope monitored 100-ohm resistor is demonstrated in figure 7. A value for KD is obtained using the following equation (refs 1 and 2):

$$KD = \text{Theta}\left(\frac{t_s}{\ln\left[1 + \left(\frac{I_F}{I_R}\right)\right]}\right) \tag{5}$$

Transition Capacitance Equation Constants

Transition capacitance equation constants Co, PHI, and N are obtained from a curve fit of transition capacitance (CJ) measured as a function of reverse junction voltage. The H.P. 9816S driven circuit used to obtain the desired data is shown in figure 8. The bias voltage depicted is supplied by the 4145B as directed by the 9816S. Voltage and capacitance values as well as measurement taking instructions are transfered to and from the 9816S microcomputer by means of the HP-IB(IEEE-488) bus. The curve fitting procedure discussed in appendix B assumes the form of the transition capacitance to be

$$CJ = \frac{Co}{(PHI - V_{CD})^N} \tag{6}$$

where V_{CD} represents the diode's junction voltage. A comparison plot between typical values of measured capacitance and a curve fit of the measured data is shown in figure 9.

Diode Model for the 1N457

The procedures described in the previous sections were implemented in the development of the following model and circuit simulation:

```
MODEL DESCRIPTION
MODEL 1N457(1-3)
ELEMENTS
CD,1-2=X1(2.3E-11/ABS(.8-VCD)**.874+1.96E-5*(JD+1.58E-10))
RB,2-3=3.45
RS,1-2=7.7E10
JD,1-2=DIODE Q(1.58E-10,22.72)
CIRCUIT DESCRIPTION
ELEMENTS
R1,2-3=100
R2,5-3=47
E1,1-2=TABLE1
E2,1-5=3
D1,3-6=MODEL 1N457
RV,6-1=100
OUTPUTS
E1,VRV,IRV
CDD1,VCDD1
FUNCTIONS
TABLE1
0,4,1E-6,4,1E-6,-7,5E-6,-7
RUN CONTROLS
INTEGRATION ROUTINE=IMPLICIT
RUN INITIAL CONDITIONS
MAX INTEGRATION PASSES = 1E30
MINIMUM STEP SIZE = 1E-30
COMPUTER TIME LIMIT = 1
STOP TIME = 5E-6
END
*EOR
8
 DBEND
```

The resulting output appears in figure 10. The results closely match the measured data depicted by figure 7. The only discrepency is the time needed for the diode current to go to zero after its junction becomes reverse biased. The difference occurs because the model does not include capacitances which exist throughout other parts of the circuit.

TRANSISTOR MODEL

The SCEPTRE transistor model (NPN) to be used is based on the Ebers-Moll model (ref 1) and appears in figure 11. The model parameters are defined as:

$$CE = \frac{Co_E}{(PHI_E - V_{CE})^{N_E}} + Theta_E\ T_E(JE + IE_S)$$

Emitter transition capacitance — Emitter diffusion capacitance

$$CE = \frac{Co_C}{(PHI_C - V_{CC})^{N_C}} + Theta_C\ TS(JC + IC_S)$$

Collector transition capacitance — Collector diffusion capacitance

Co_E = Constant of the emitter transition capacitance equation

Co_C = Constant of the collector transition capacitance equation

PHI_E = Emitter base junction contact potential

PHI_C = Collector base junction contact potential

JE = Current generator representing the emitter base junction

$JE = IE_S[EXP(Thets_E\ V_{CE}) - 1]$

JC = Current generator representing the collector base junction

$JC = IC_S[EXP(Theta_C\ V_{CC}) - 1]$

N_E = Emitter junction grading constant

N_C = Collector junction grading constant

JN = Currect generator dependent on the emitter base junction current

$JN = \alpha_N\ JE$

JI = Current generator dependent on the collector base junction current

$JI = \alpha_I\ JC$

IE_S = Emitter-base saturation current measured in the active region

IC_S = Collector-base saturation current measured in the active region

$Theta_E$ = Constant of the emitter base junction equation

$Theta_C$ = Constant of the collector base junction equation

TE = Time constant of the emitter diffusion capacitance equation

$$TE = \frac{1}{6.28\ F_N}$$

TS = Time constant of the collector diffusion capacitance equation

$$TS = \frac{1}{6.28\ F_I}$$

F_N = The average f_t normal

F_I = The average f_t inverse

TCI = Charge control parameter related to storage time

α_N = Forward current gain = $\frac{I_C}{I_E}$

α_N is entered as a function of JE in the SCEPTRE model.

α_I = Inverse current gain = $\frac{I_E}{I_C}$

α_I is entered as a function of JC in the SCEPTRE model.

RB = Base bulk resistance

RC = Collector bulk resistance

R1 = Emitter-base junction leakage resistance

R2 = Collector-base junction leakage resistance

Junction Constants and Saturation Currents

Constants $Theta_E$ and $Theta_C$ represent values for the base-to-emitter and base-to-collector junction constants, respectively. Similarly, parameters IE_S and IC_S represent base-to-emitter and base-to-collector saturation currents. These values are determined in the same way as in the diode case. The test setup used to obtain the forward chacteristic of the base-to-emitter junction is shown in figure 12, while the circuit used to obtain the characteristic of the base-to-collector junction is depicted in figure 13. An active region collector-to-emitter voltage on the order of that seen by the transistor during application should be applied by SMU2 during this test. In this test, SMU2 acts as a voltage source in series with a current monitor. Physical connections between the transistor under test and the HP4145B take place by means of an HP16058A test fixture. The fixture and its connections for the transistor case are depicted in appendix A.

Forward and Inverse Current Gains

Forward current gain (α_N) and inverse current gain (α_I) are defined by reference 1 as follows:

$$\alpha_N = \frac{I_C}{I_E} \quad \text{and} \quad \alpha_I = \frac{I_E}{I_C} \qquad (7 \text{ and } 8)$$

α_N is obtained from the data measured by the circuit of figure 12 while determination of α_I is based on the results of the test setup of figure 13. α_N and α_I are determined for different values of I_E and I_C, respectively, allowing them to be described within the model in a tabular way as functions of current.

Emitter and Collector Transition Capacitances

As with the junction constants and saturation currents previously discussed, the emitter and collector transition capacitance parameters (N_E, Co_E, PHI_E, N_C, Co_C, PHI_C) are also determined as in the diode case. The test circuits for each junction appear in figures 14 and 15.

Base and Collector Bulk Resistance

Bulk resistance (RB) is obtained from the base-to-emitter forward characteristic. Its determination is the same as in the diode case. Collector bulk resistance will be assumed to be typically on the order of 1 ohm. A more precise value for RC can be obtained by methods described in reference 1.

Junction Leakage Resistances

The base-to-emitter leakage resistance (R1) and collector-to-base leakage resistance (R2) are obtained from the junction reverse bias characteristics. The procedure is the same as in the diode case. The test setups used are described in figures 16 and 17. In these cases, SMU1 acts as a current source and voltage meter while SMU3 supplies a voltage of zero and measures the junction's current.

Time Constant of the Emitter Diffusion Capacitance Equation

Parameter TE is the emitter diffusion time constant and is introduced in an attempt to describe, in terms of a time constant, the capactive effect which is observed in the transistor's emitter junction as a function of forward base-to-emitter voltage. The development of such a relationship begins by expressing junction voltage in terms of parameter TE. This is done by equating the exponetial product of $Theta_E$ and VC_E of the equation for current generator JE to the familiar exponential term of time divided by some time constant. In this case, the time constant will be called TE and will produce the following expression for junction voltage:

$$VC_E = \frac{t}{Theta_E \; TE} \qquad (9)$$

An expression for the emitter diffusion capacitance (CE_D) as a function of TE can now be developed. Since capacitance is defined as

$$C = \frac{I}{\frac{dV}{dt}} \tag{10}$$

the derivative of equation 9 with respect to time can be subsituted into equation 10 yielding the following expression for capacitance CE_D:

$$CE_D = \frac{I_{CE_D}}{\frac{1}{Theta_E\ TE}} = Theta_E\ TE\ (JE + IE_S) \tag{11}$$

The above expression describes the relationship between capacitance CE_D and parameter TE. Values for CE_D can now be determined once parameter TE is defined. With this in mind, an expression for TE is next developed from the charge voltage relationship across capacitor CE_D. Starting with the charge voltage relationship across a capacitor

$$Q_E = CE_D\ V_{CE_D} \tag{12}$$

where Q_E is the charge on the junction diffusion capacitance CE_D with voltage V_{CE_D} across it. Since a determination of TE would be most desirable in terms of emitter current, it is necessary to rewrite equation 12 as follows:

$$Q_E = CE_D\ I_E\ RE \tag{13}$$

where I_E is the emitter current of the transistor and RE is the equivalent emitter junction resistance seen by current generator JE and dimensionally equal to $1/Theta_E(JE + IE_S)$. Differentiating both sides of equation 13 with respect to I_E yields

$$\frac{dQ_E}{dI_E} = CE_D\ RE = \frac{CE_D}{Theta_E\ (JE + IE_S)} = TE \tag{14}$$

The term $\frac{dQ_E}{dI_E}$ has the units of a time constant and can be seen from equation 11 to be equal to the emitter diffusion time constant TE. Through the use of this definition and the equation of charge continuity (eq 15), an expression for TE can be developed in terms of emitter current and time

$$I_B = \frac{dQ_E}{dt} + \frac{Q_B}{\tau_B} \tag{15}$$

The above equation states that the base current of the transistor is made up of the recombination of excess carriers every λ_B seconds and the time varying change in excess carrier distribution. By separating variables and then inverting each side of the equation,

$$\frac{1}{I_B - \frac{Q_B}{\lambda_B}} = \frac{dt}{dQ_E} \tag{16}$$

By multiplying through by dI_E, substituting $\frac{dQ_E}{TE}$ for dI_E on the right side of the equation, and then integrating, a solution for TE in terms of I_E can be obtained as follows:

$$\int_{27\%I_E}^{73\%I_E} \frac{dI_E}{I_{B1} - \frac{Q_B}{\lambda_B}} = \int_0^{tr} \frac{dt}{dQ_E} \times \frac{dQ_E}{TE} = \int_0^{tr} \frac{dt}{TE} \tag{17}$$

Limit t_r represents the time it takes for the emitter current to rise form 27% to 73% of its final value. I_B is assumed to go from zero to I_{B1} in a stepwise manner. Since $\frac{Q_B}{\lambda_B}$ represents the d.c. component of the base current, it can be subsituted by the d.c. emitter current divided by $\beta + 1$ as follows:

$$(\beta + 1) \int_{27\%I_E}^{73\%I_E} \frac{dI_E}{(\beta + 1) I_{B1} - I_E} = \int_0^{tr} \frac{dt}{TE} \tag{18}$$

β is the average β for the 27% to 73% collector current transition experienced. Values of β for different values of collector current can be calculated from the α_N results obtained from equation 7 and the following expression for β .

$$\beta = \frac{\alpha_N}{(1 - \alpha_N)} \tag{19}$$

Integrating, the following is obtained:

$$\frac{t_r}{TE} = -(\beta + 1) \ln[(\beta + 1) I_{B1} - I_E] \Big|_{27\%I_E}^{73\%I_E} \tag{20}$$

By evaluating equation 20 over the limits indicated and then substituting I_E for $(\beta + 1) I_{B1}$, the following expression for TE can be developed:

$$TE = \frac{t_r}{(\beta + 1) \ln \frac{0.73}{0.27}} \approx \frac{t_r}{\beta + 1} \qquad (21)$$

Therefore, the value of TE for different saturation currents can be obtained by measuring the time necessary for the collector current or collector-to-emitter voltage of the transistor to go from 27% to 73% of its final value. Therefore, TE is expressed within the model in a tabular manner as a function of current generator JE and is obtained from the test setup of figure 18. An example of the oscilloscope trace generated by the test circuit of figure 18 is shown in figure 19.

Time Constant of the Collector Diffusion Capacitance Equation

The time constant (TS) of the collector diffusion capacitance equation is determined by observng the depletion of excess charge in the transistor's base region as it is brought out of saturation. By using the equation of charge continuity, reference 3 develops an expression for the transistor's storage time constant as a function of base current and collector saturation current. The expression is as follows:

$$\lambda_S = \frac{dQ_{BS}}{dI_B} = \frac{t_s}{\ln \left(\frac{(I_{B1} - I_{B2})}{I_C/B - I_{B2}} \right)} \qquad (22)$$

In the above expression, I_{B1} represents the base current while the transistor is in saturation; I_{B2}, the base current used to bring the transistor out of saturation; and I_C, the collector saturation current. Parameter t_s is the storage time needed to deplete the base of excess charge carriers and begin to bring the transistor out of saturation. Values for I_{B1}, I_{B2}, and t_s can be obtained by using the circuit of figure 18. The method used to obtain a measurement for t_s is shown in figure 19. Parameter t_s is measured from the time when the transistor's base is at its minimum to the time its collector voltage reaches 10% of its final value. The 10% point of reference is used to make it easier to obtain a reading while introducing only a negligible amount of error into the measurement. The result of equation 22 and the inverse mode model components JC, CC, and JI of figure 10 are used to explain saturation region behaviour and develop time constant TS in terms of current generator JC. TS is defined as:

$$TS = \frac{dQ_{BS}}{dI_B} = \frac{t_s}{\ln \left(\frac{(I_{B1} - I_{B2})}{I_C/B - I_{B2}} \right)} \times \frac{\alpha_I}{\beta_I} \qquad (23)$$

Parameters β_N, β_I, I_C, and α_I are all functions of the operating point and are obtained by a SCEPTRE simulation (ref 1). The simulation consists primarily of a constant capacitance steady state model of the transistor which uses all of the parameters obtained up to this point. The model is excited in a common emitter

circuit at different values of collector current. The results produce values from which parameter TS can be expressed in tabular form as a function of the model current generator JC.

A Transistor Model for the 2N2222

The procedures described in the previous sections were implemented in the development of a model for the 2N2222 transistor. Tabulated test results used in the determination of parameters TE and TS appear in tables 1 and 2, respectively. A listing of the model and the SCEPTRE input used to simulate the circuit of figure 18 follow:

```
MODEL DESCRIPTION
MODEL 2N2222(B-E-C)
ELEMENTS
CE,1-E=Q1(4.5E-11,.75,VCE,.78,28,T3(JE),JE,2.2E-11)
CC,1-2=Q1(2.9E-11,.75,VCC,1.03,28.4,T4(IC),JC,2.8E-11
RB,B-1=47
RC,C-2=.5
R1,1-E=3.9E10
R2,1-2=1.1E10
JE,1-E=DIODE Q(2.2E-11,28)
JC,1-2=DIODE Q(2.8E-11,28.4)
JN,2-1=TABLE1(JE)*JE
JI,E-1=TABLE2(JC)*JC
FUNCTIONS
Q1(A,B,C,D,E,F,G,H)=(A/ABS(B-C)**D+E*F*(G+H)
TABLE1=0,.9925,4.1E-4,.9925,1.1E-3,.9928,2.35E-3,.9926,1.04E-2,
.9926,1.15E-2,.9913,1.37E-2,.992,2E-2,.992
TABLE2=0,5.036E-2,2.019E-6,5.036E-2,2.67E-5,.1028,5.33E-5,.1386,
8.136E-5,.166,1.244E-4,.197,2.6E-4,.2615,3E-4,.2615
TABLE3=0,.5E-9,15E-3,.5E-9,20E-3,.42E-9,30E-3,.5E-9,40E-3,.833E-9,
1,.833E-9
TABLE4=0,105.7E-9,5.34E-4,105.7E-9,1.117E-3,117E-9,2.44E-3,58.6E-9
1,58.6E-9
CIRCUIT DESCRIPTION
ELEMENTS
R1,2-3=1E3
R2,5-4=100
E1,1-2=TABLE1
E2,1-5=4
T1,3-1-4=MODEL 2N2222
J1,4-1=0
OUTPUTS
V.J1,E1
FUNCTIONS
TABLE1
0,-1.6,1200E-9,-1.6,1280E-9,1.6,2480E-9,1.6,2520E-9,-1.6,2600E-9,-1.6
RUN CONTROLS
INTEGRATION ROUTINE=IMPLICIT
RUN INITIAL CONDITIONS
MAX INTEGRATION PASSES = 1E30
```

```
MINIMUM STEP SIZE = 1E-30
COMPUTER TIME LIMIT = 1
STOP TIME =4000E-9
END
*EOR
8
 DBEND
```

Its resulting output appears in figure 20. The results closely match the measured data depicted by figure 19.

CONCLUSIONS

The results obtained in this report confirm the modeling procedures used by Bowers and Sedore and demonstrate a method for successfully automating those procedures using the Hewlett Packard 9816S microcomputer and 4145B semiconductor parameter analyzer.

Table 1. Transistor current rise time parameters for the 2N2222

I_C (mA)	t_r (ns)	?	T_E (ns)
40	100	120	0.833
30	60	120	0.500
20	50	120	0.420
15	60	120	0.500

Table 2. Transistor storage time parameters for the 2N2222

V_{in} (V)	V_B (V)	I_{B1} (mA)	I_{B2} (mA)	I_{Csat} (mA)	IC (mA)	t_S (ns)	TS (ns)
1.5	0.8	0.7	-2.3	40	0.53	20	105.7
2.0	0.8	1.2	-2.8	40	1.17	40	117.0
3.0	0.8	2.2	-3.8	40	2.44	30	58.6

B_N = 124 B_I = 0.354

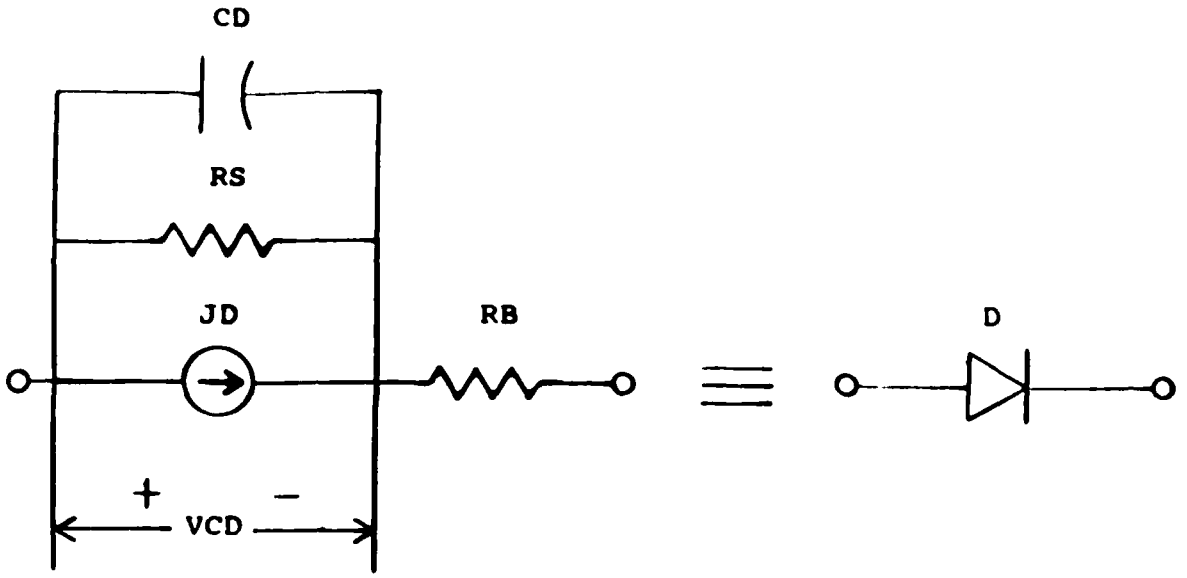


Figure 1. SCEPTRE diode model

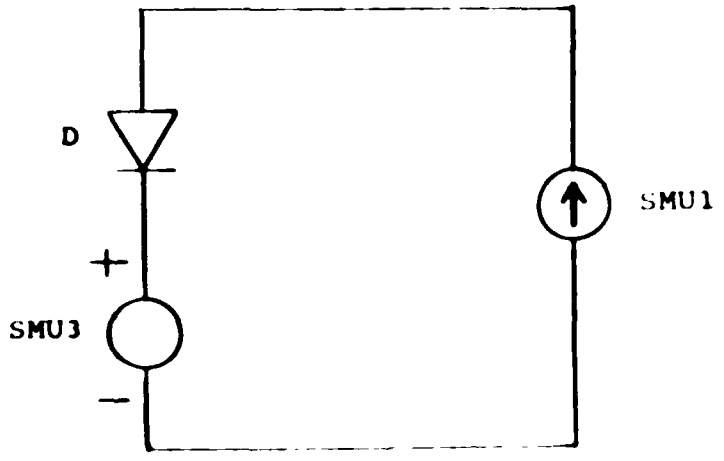


Figure 2. Forward diode characteristics test circuit

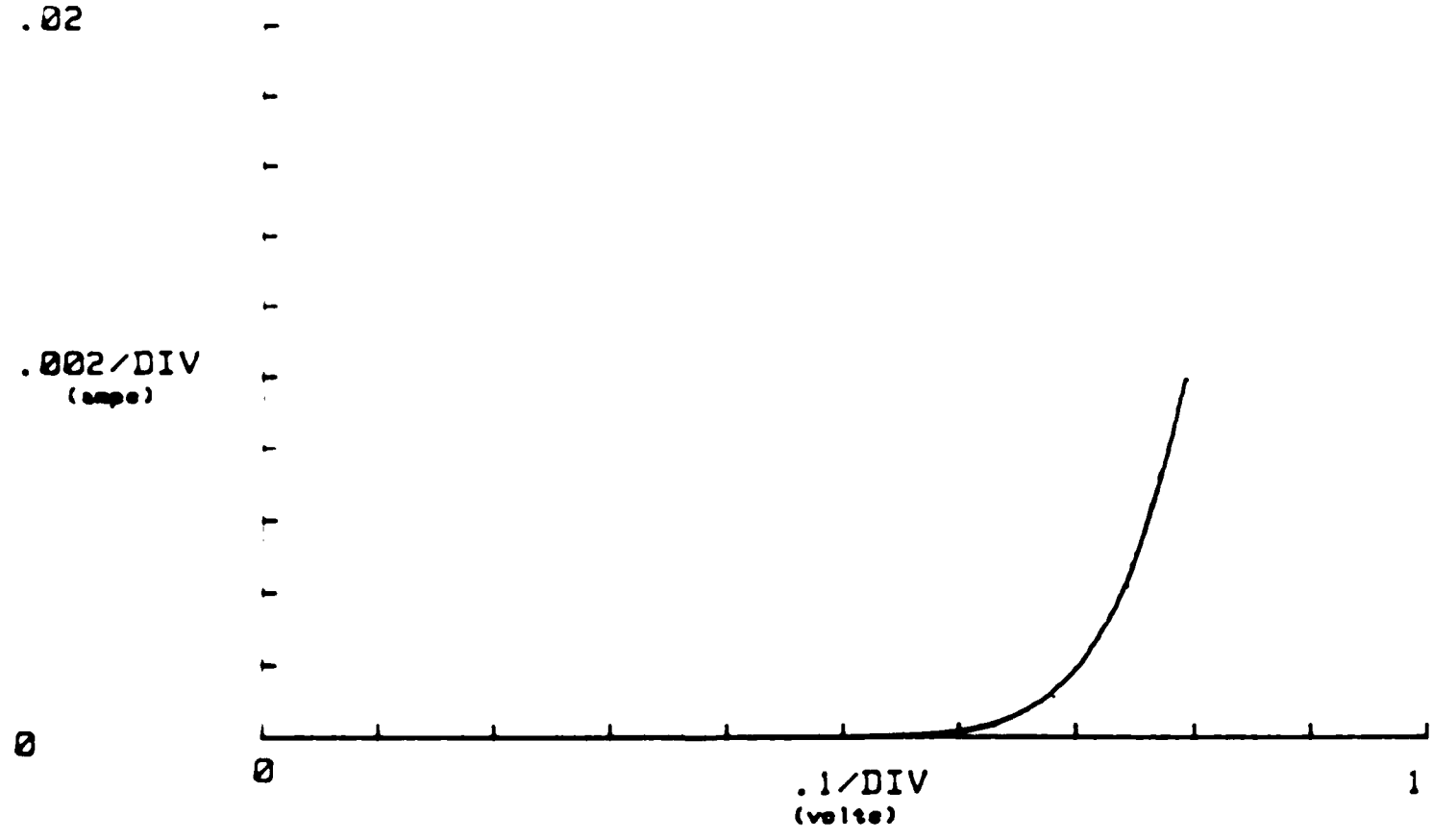


Figure 3. Forward diode characteristic of a 1N457

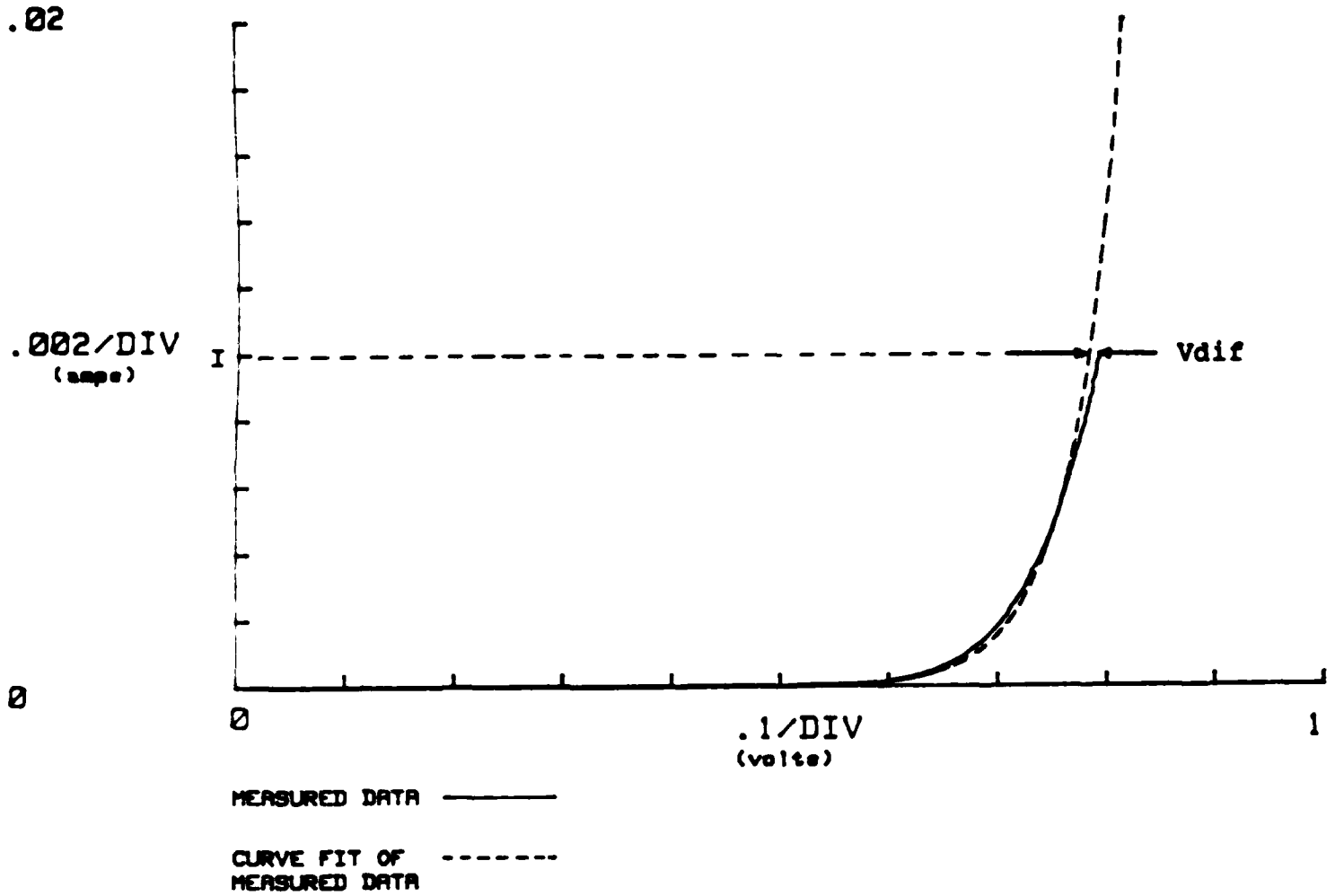


Figure 4. Curve fit of the forward characteristic of a 1N457

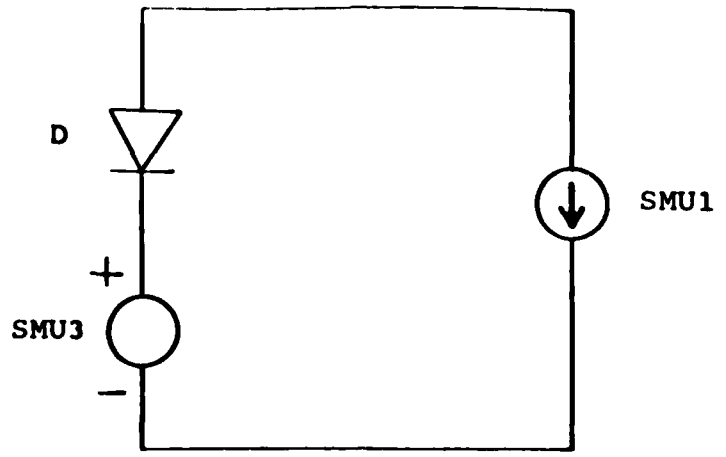


Figure 5. Reverse diode characteristic test circuit

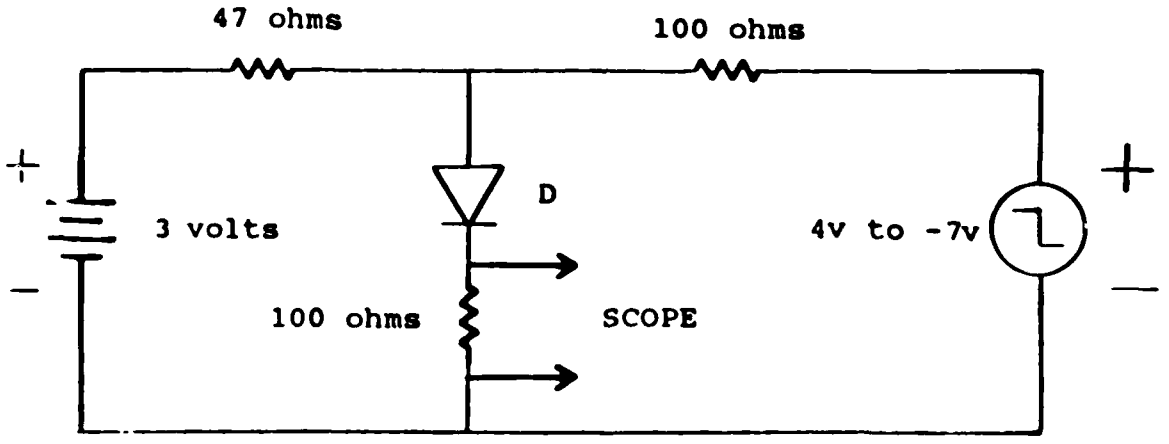


Figure 6. Diffusion capacitance test circuit

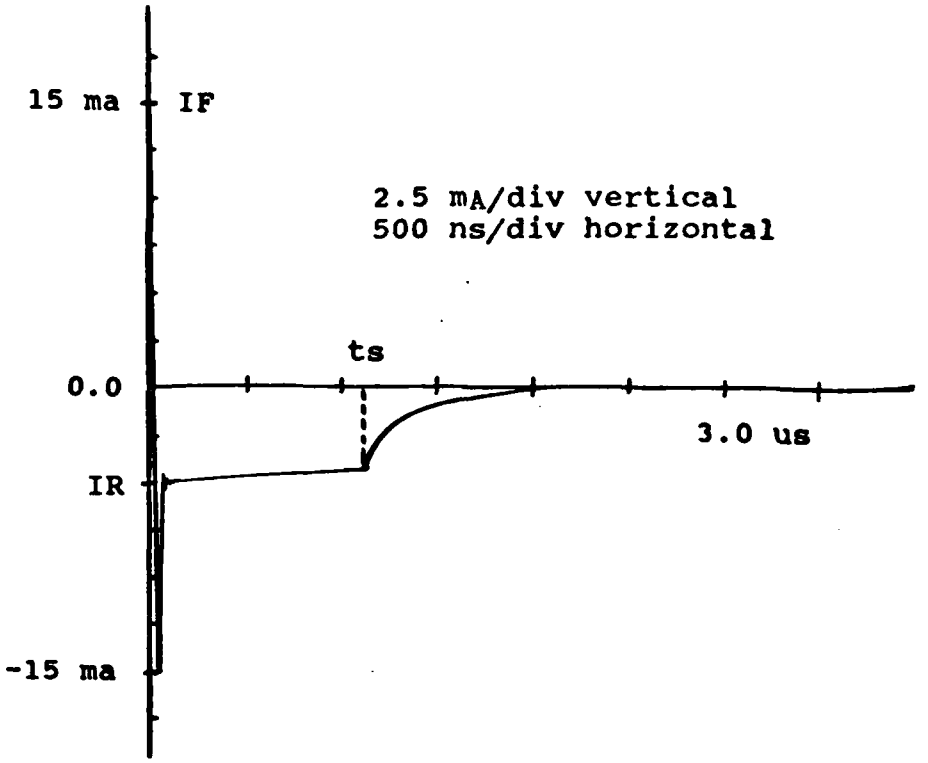


Figure 7. Diode (1N457) reverse recovery waveform from the test setup of the diffusion capacitance test circuit

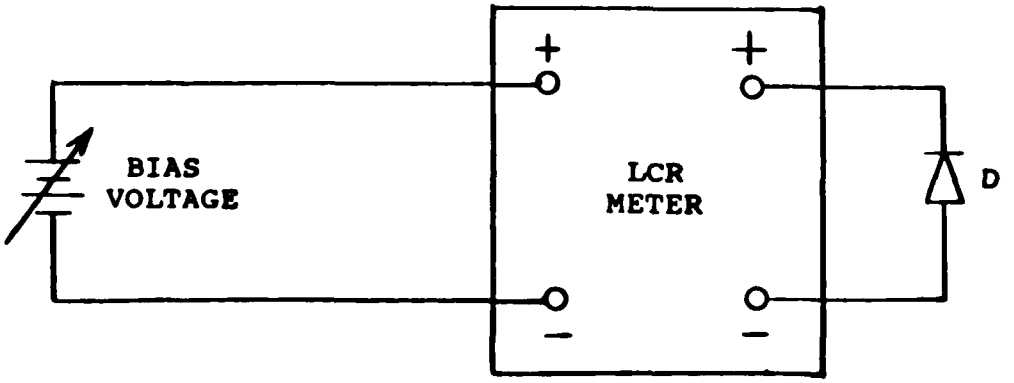


Figure 8. Transition capacitance test circuit

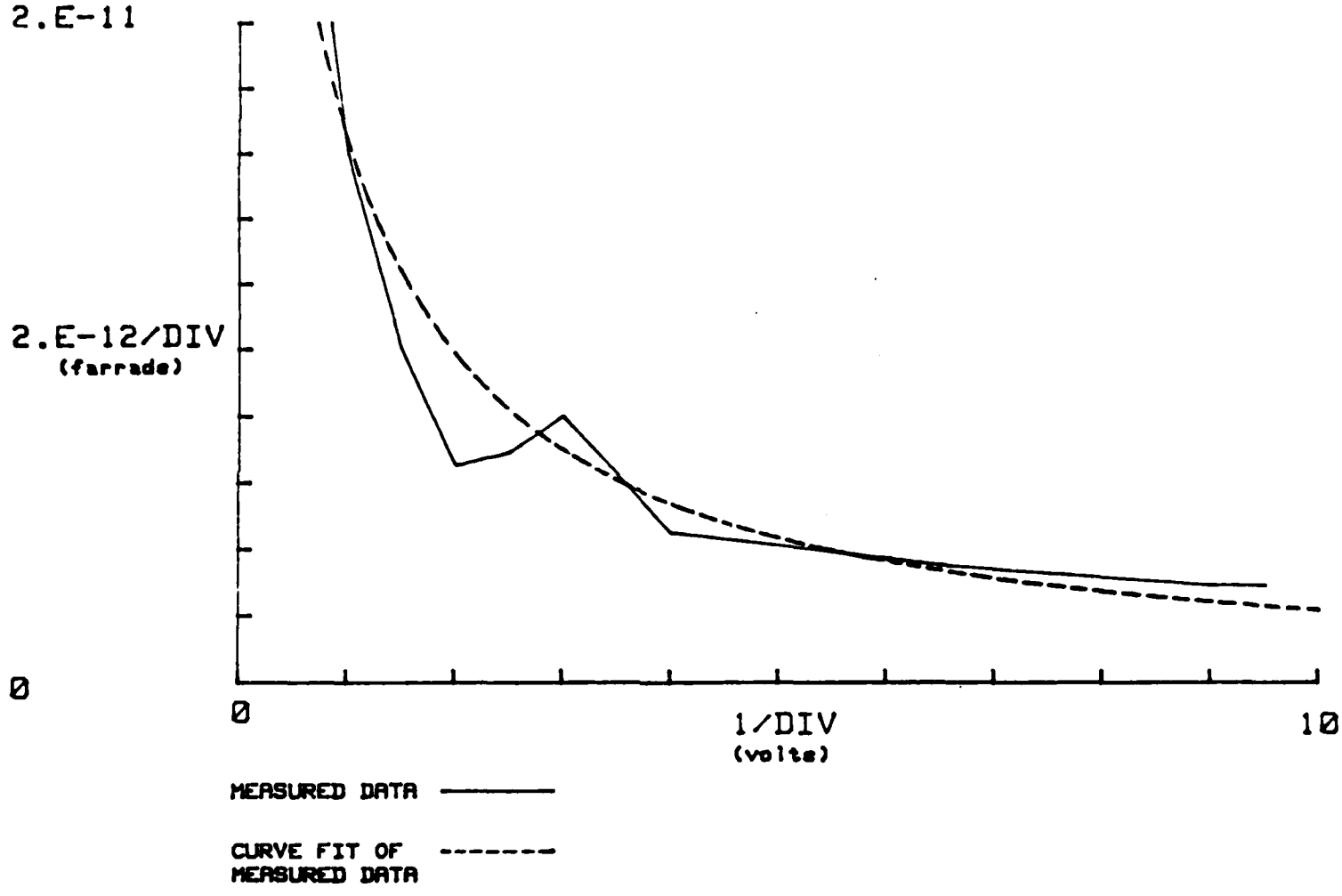


Figure 9. Transition capacitance of diode 1N457 as a function of reverse function voltage

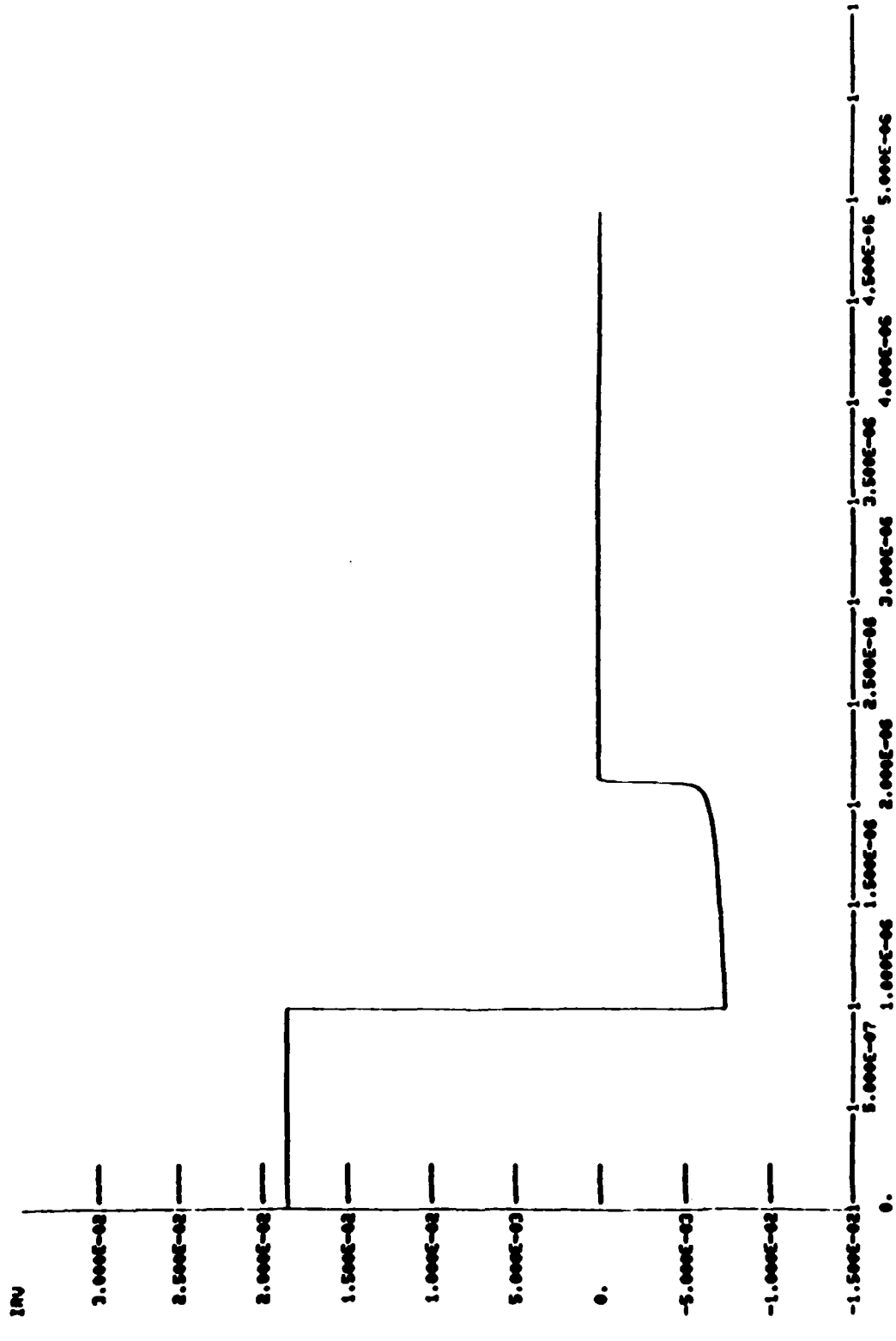


Figure 10. Simulated diode current of the diffusion capacitance test circuit

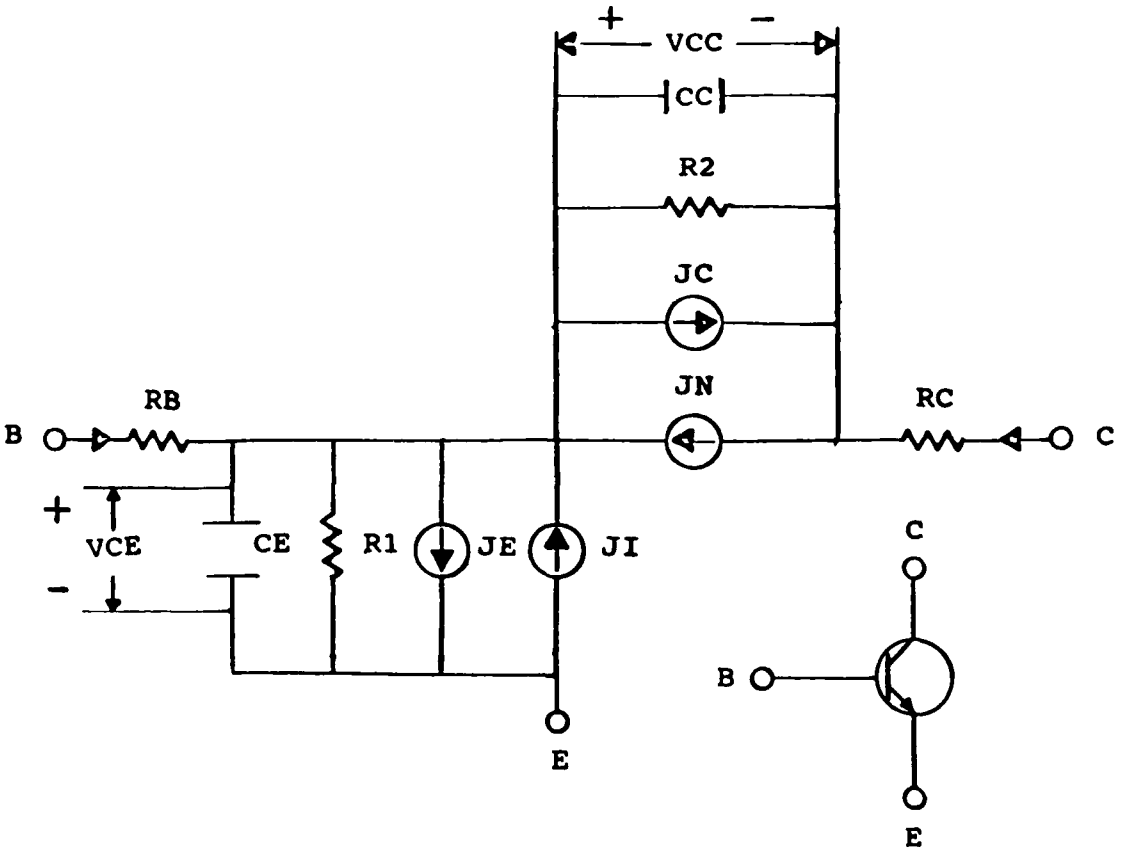


Figure 11. SCEPTRE NPN transistor model

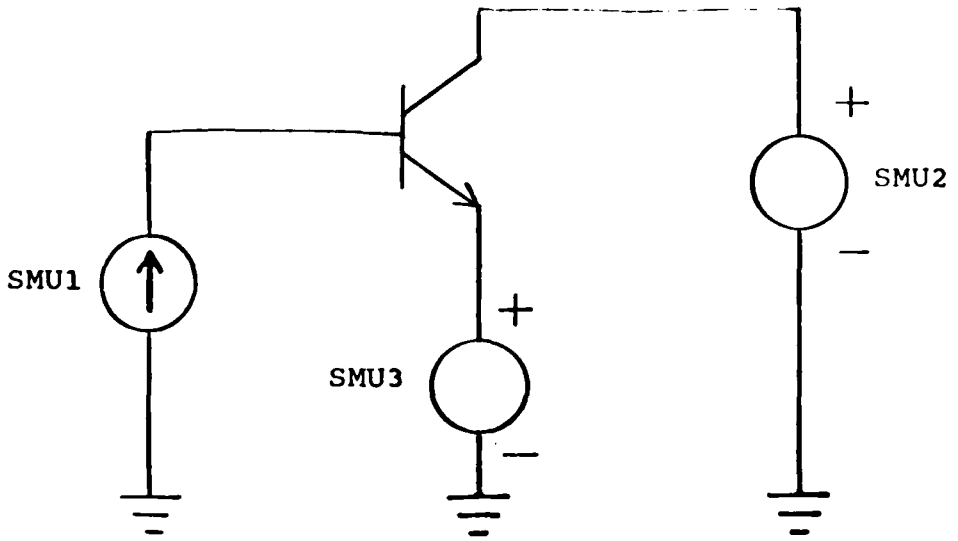


Figure 12. Base-to-emitter forward characteristic test circuit

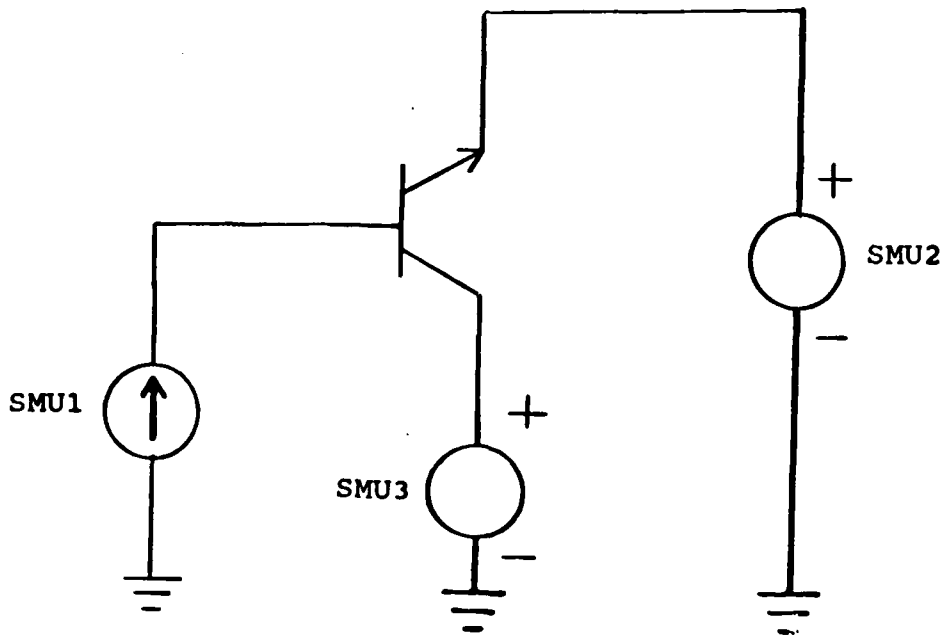


Figure 13. Base-to-collector forward characteristic test circuit

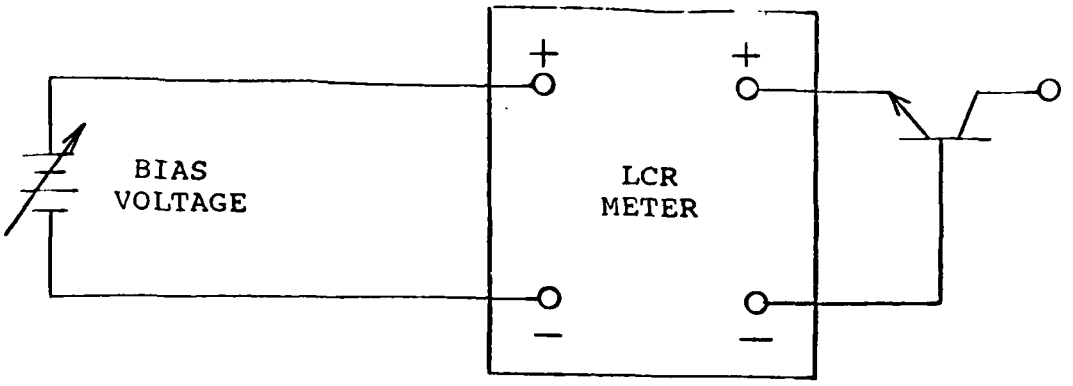


Figure 14. Base-to-emitter transition capacitance test circuit

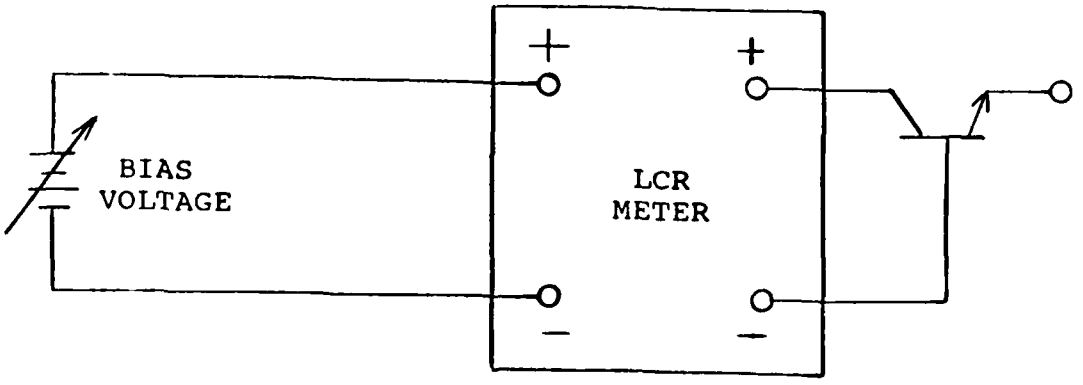


Figure 15. Base-to-collector transition capacitance test circuit

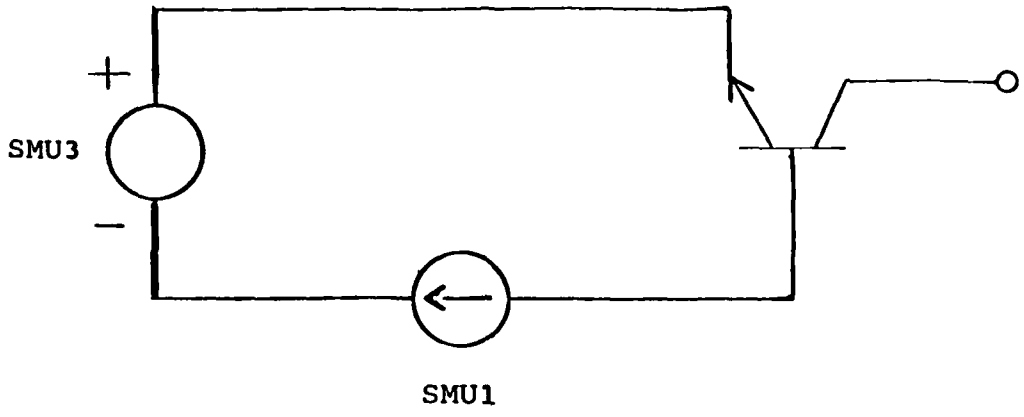


Figure 16. Base-to-emitter reverse characteristic test setup

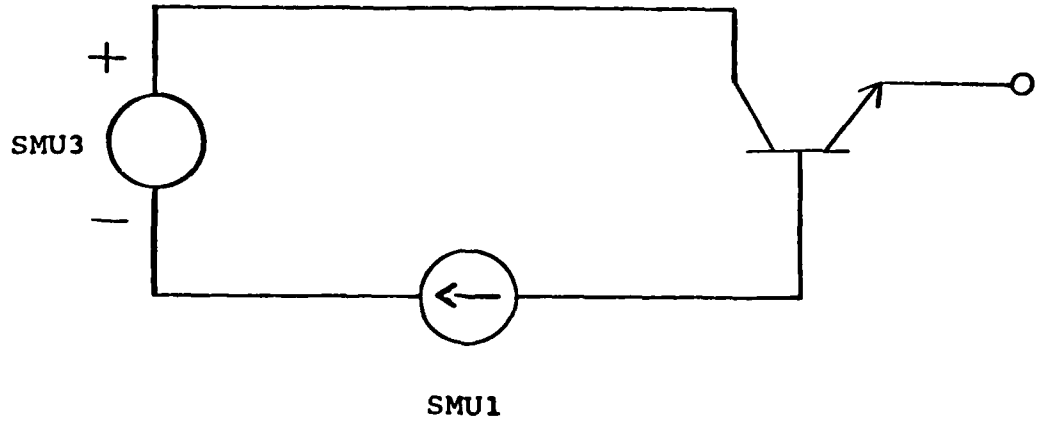


Figure 17. Base-to-collector reverse characteristic test setup

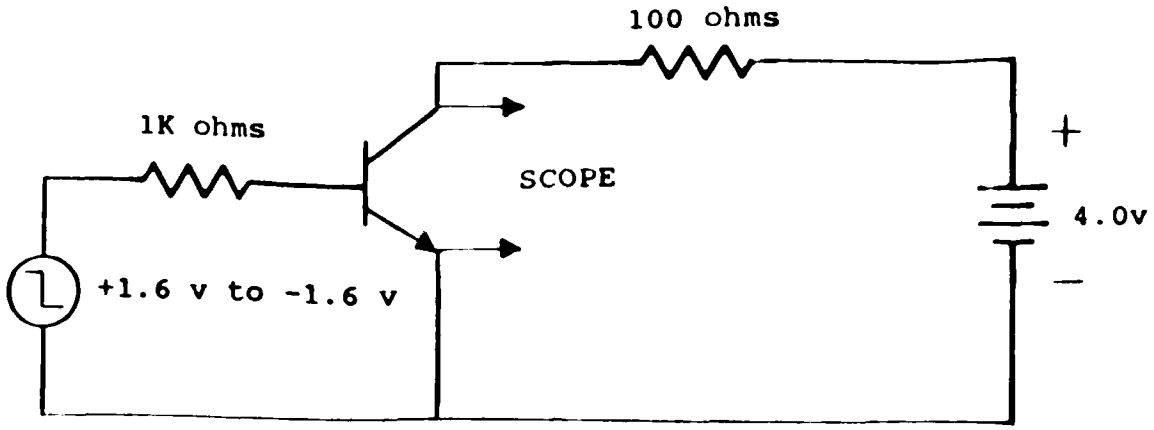


Figure 18. Rise time test circuit

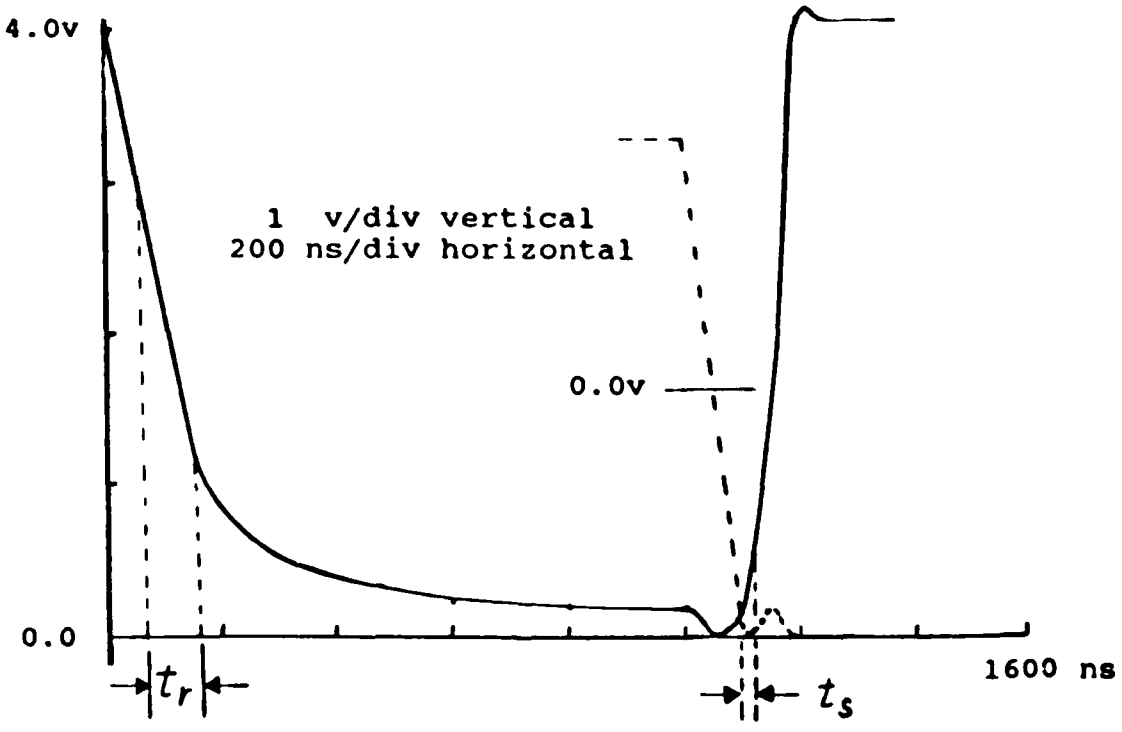
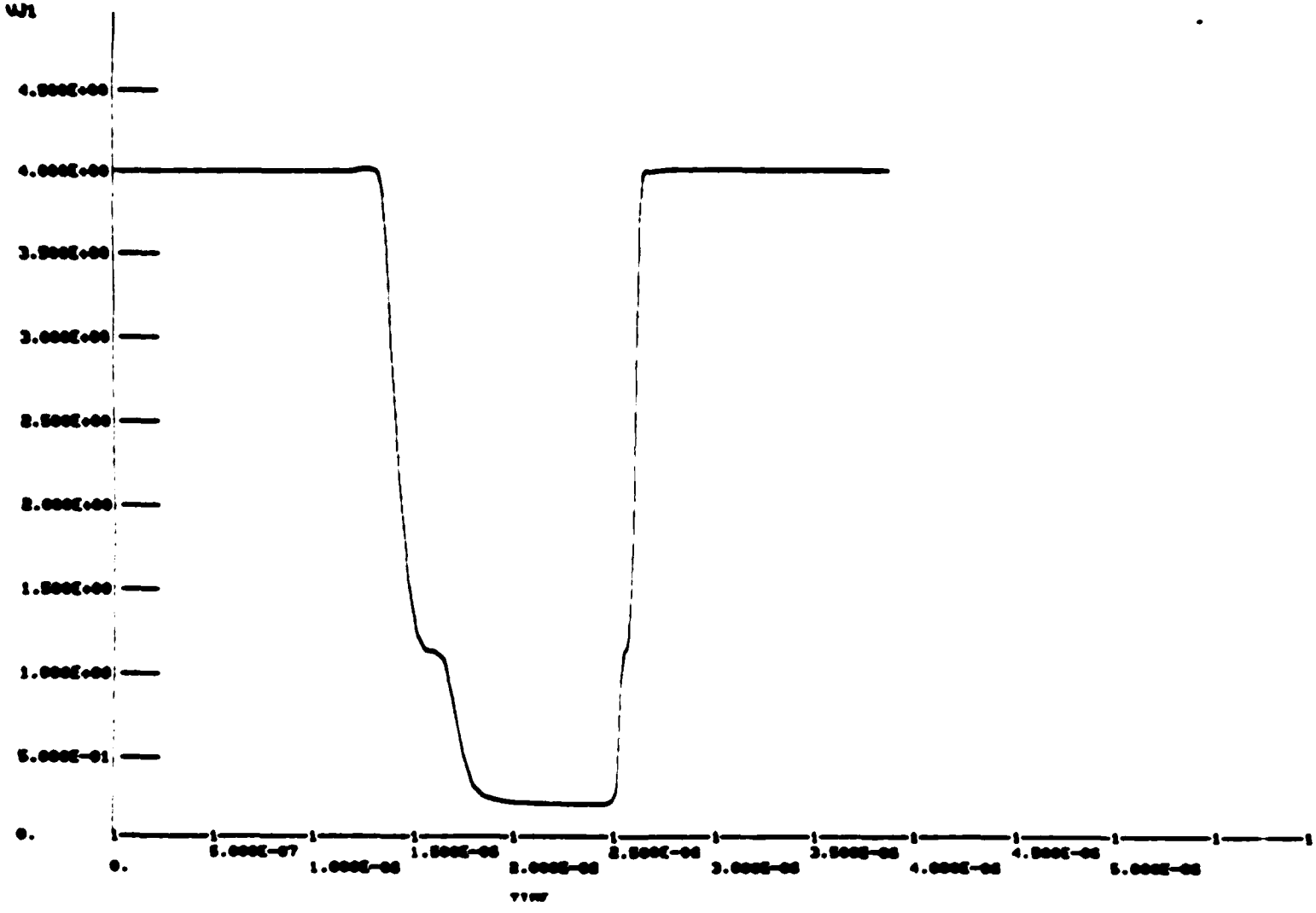


Figure 19. Oscilloscope output of rise time test circuit


VM
4.000E+00
4.000E+00
3.500E+00
3.000E+00
2.500E+00
2.000E+00
1.500E+00
1.000E+00
5.000E-01
0.
0.
5.000E-07
1.000E-06
1.500E-06
2.000E-06
2.500E-06
3.000E-06
3.500E-06
4.000E-06
4.500E-06
5.000E-06
TIME

REFERENCES

1. Bowers, James C. and Sedor, Stephen R., "SCEPTRE: A Computer Program for Circuit and Systems Analysis," Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1971

2. Streetman, Ben G., Solid State Electronic Devices, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, pp 170-176, 1980.

3. Phillips, Alvin B., Transistor Engineering, McGraw-Hill, New York, N.Y., pp 341-346, 1962.

4. Barnas, Robert E., Cuvit II - A Curve Fitting Program with Plotting Options, Management Information Systems Directorate, Picatinny Arsenal, Dover, NJ.

APPENDIX A

HP16058A TEST FIXTURE LAYOUTS AND EQUIPMENT LIST

Physical connections between the devices under test and the HP4145B semiconductor parameter analyzer are discussed in this appendix. Connections are made through the use of an HP16058A test fixture. The wiring layouts used in the diode and transistor tests are demonstrated in figures A-1 and A-2. A general list of the equipment used in this report is shown in table A-1.

While acting as an interface between the HP4145B and the device under test (DUT), the test fixture also provides a means of easily modifying circuit connections with the use of a connection switch. The switch in figures A-1 and A-2 connects the center column nodes (COMM) to the nodes of either columns 1 or 2.

When performing diode related tests, the layout of figure A-1 is used. The connection switch is moved to position 1 when the diode's forward characteristic and leakage resistance are being determined. The switch is moved into position 2 when transition capacitance tests are being performed, but the diode must be removed from the test fixture in this case and connected directly to the LCR meter.

Transistor tests are made using the layout of figure A-2. Once again, the connection switch is used to modify test procedures without disturbing the test fixture. The switch is placed in position 1 when performing the forward NORMAL mode characteristic test and in position 2 when determining the INVERSE mode characteristic. Transition capacitance tests are made using the layout of figure A-1 while remembering that the diode depicted represents the transistor junction under test. Junction leakage resistance tests use the layout of figure A-2 with modifications stipulated by base-to-emitter and base-to-collector reverse characteristic test setups described earlier in this report.

Table A-1. Equipment list

1. Hewlett Packard 9816S microcomputer.
2. Hewlett Packard 4145B semicoductor parameter analyzer.
3. Hewlett Packard 4262A LCR meter.
4. Lambda LE103 FM power supply.
5. Tektronix 5441 storage oscilloscope.
6. Tektronix FG504 function generator.

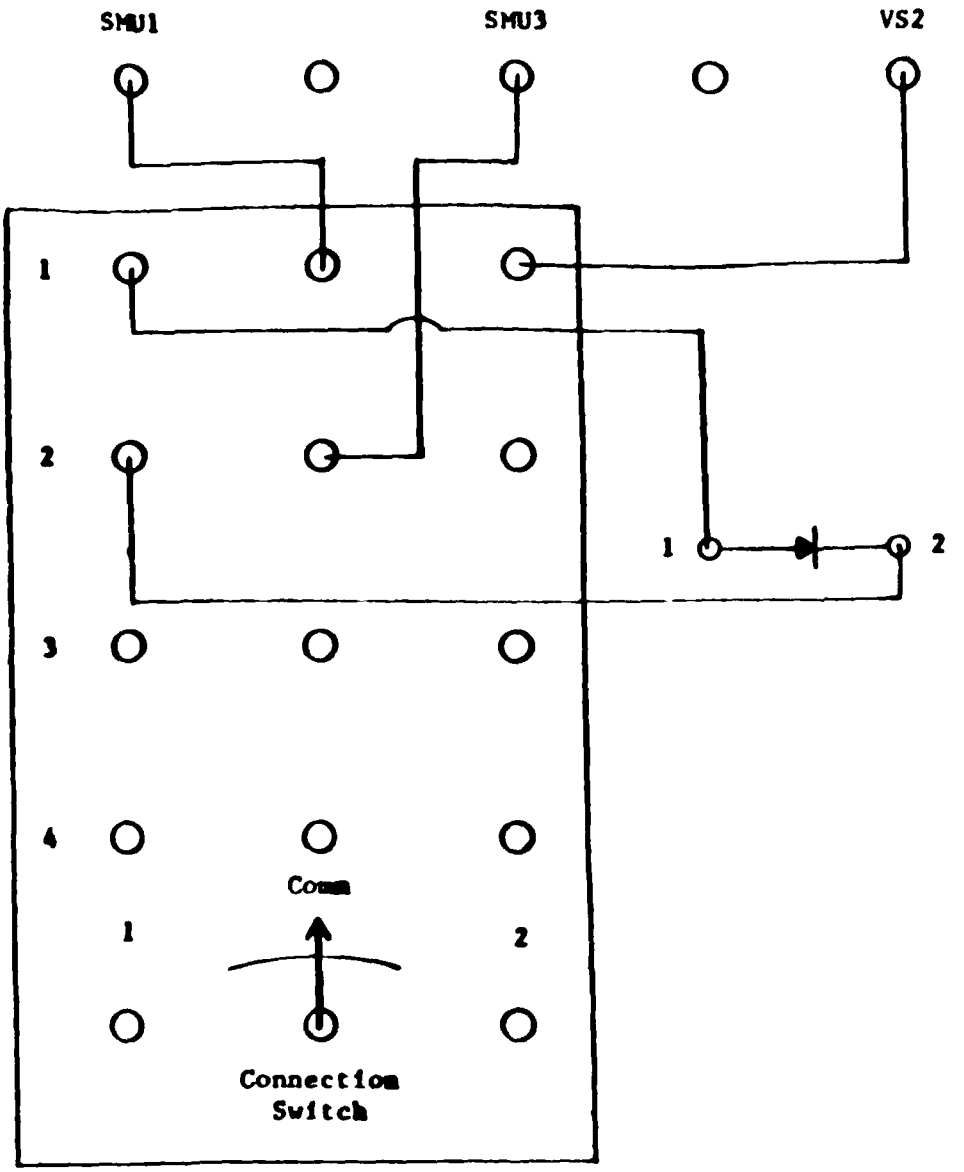


Figure A-1. Test fixture (H.P. 16058A) diode layout

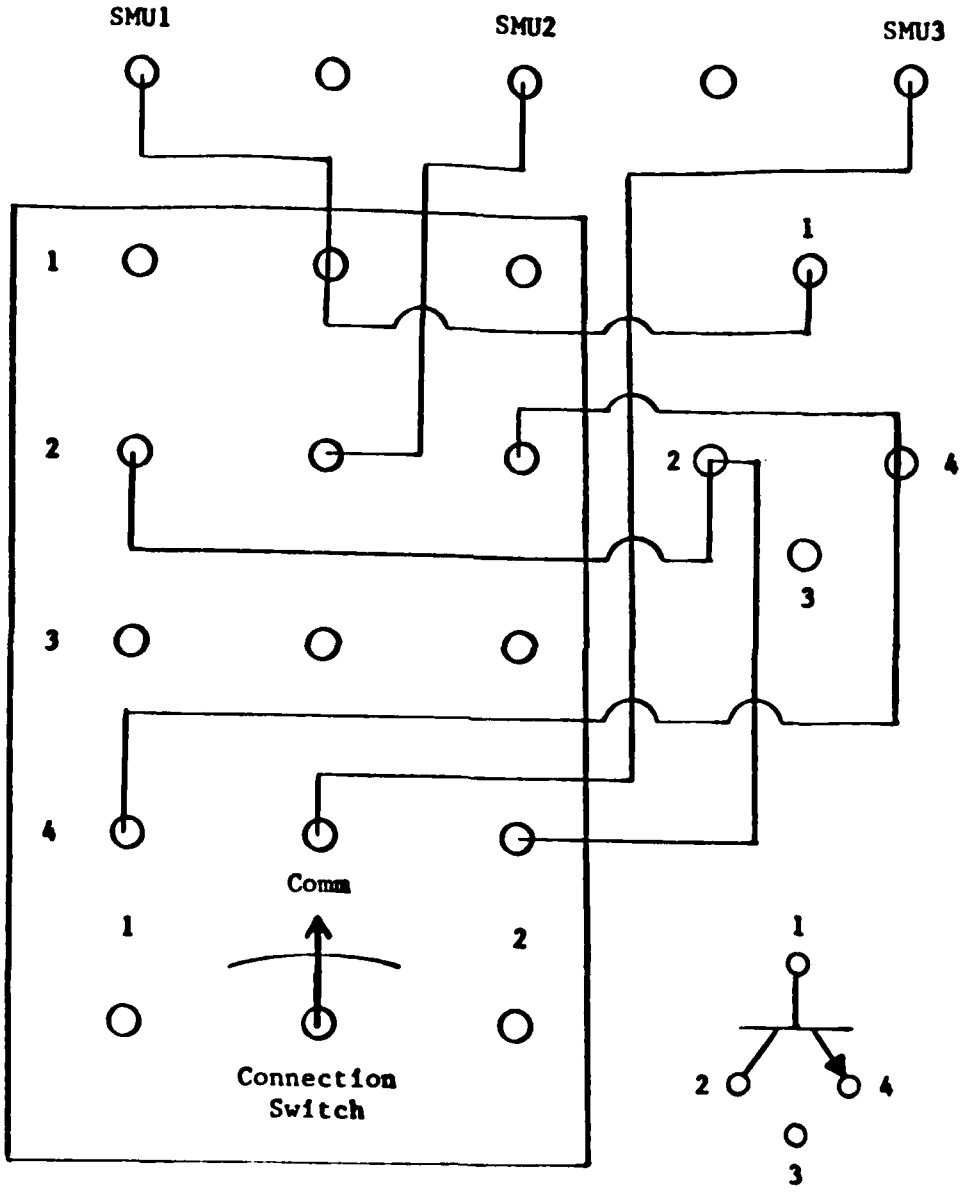


Figure A-2. Test fixture (H.P. 16058A) transistor layout

APPENDIX B

LEAST-SQUARES CURVE FITTING

The curve fitting method used in this report is known as the least-squares method.* It is based upon the concept that the best line fitted to a set of data points is the one for which the sum of the squares of the deviations between the points and the line is a minimum.

The deviations are squared to eliminate the possible cancelling of positive and negative deviations at different points which could give a false impression of a good fit.

This report maps all of the expressions to be used for fitting purposes to the form of the straight line, $Y = A + BX$. The sum of the squares of the deviations may be expressed as

$$\sum (y_c - y_o)^2 = \sum (A + Bx_o - y_o)^2 \qquad (B\text{-}1)$$

where $y_c = A + Bx_o$ is the calculated ordinate for the value of $x = x_o$.

The values of the constants, A and B, for which this expression is a minimum may be determined by finding the partial differentiation of equation B-1 with respect to each constant and then setting it equal to zero.

For A:

$$\frac{\partial}{\partial A} \sum (A + Bx_o - y_o)^2 = 0$$

$$2 \sum (A + Bx_o - y_o) = 0$$

$$\sum (A + Bx_o - y_o) = 0$$

For B:

$$\frac{\partial}{\partial B} \sum (A + Bx_o - y_o)^2 = 0$$

$$2 \sum (Ax_o + Bx_o^2 - x_o y_o) = 0$$

$$\sum (Ax_o + Bx_o^2 - x_o y_o) = 0$$

These two equations can be solved simultaneously for unique values of the quantities A and B since values of x_o and y_o are available from the original data. The two equations may be written in the form:

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* Barnas, Robert E., Cuvit II - A Curve Fitting Program with Plotting Options, Management Information Systems Directorate, Picatinny Arsenal, Dover, NJ.

$$\sum y_o = \sum A + \sum Bx_o$$

$$\sum x_o y_o = \sum Ax_o + \sum Bx_o^2$$

Factoring A and B from the terms gives

$$\sum y_o = N\,A + B \sum x_o$$

$$y_o x_o = A \sum x_o + B \sum x_o^2$$

where N = number of data points and finally

$$A = \frac{\sum x_o \quad x_o y_o - \sum y_o \sum x_o^2}{(\sum x_o)^2 - N \sum x_o^2}$$

$$B = \frac{\sum y_o \sum x_o - N \sum x_o y_o}{(\sum x_o)^2 - N \sum x_o^2}$$

The manner in which assumed data forms were mapped into the straight line form is described in table B-1.

Table B-1. Straight line equation mappings used in the least-squares fit of semiconductor data

Equation no.	Original form	Desired form	Mapping
2	$I=I_S\ \mathrm{Exp}(\mathrm{Theta}\ V_{CD})$	Y=A+BX	Y=ln(I) A=ln(I_S) B=Theta X=V
4	$I=\frac{V}{RS}$	Y=A+BX	Y=I A=0 B=$\frac{1}{RS}$ X=V
6	$CJ=\frac{Co}{((PHI-VJ)^N)}$	Y=A+BX	Y=ln(CJ) A=ln(Co) B=-N X=ln(PHI-VJ)

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